Cyrix® Advancing the Standards

Technical Brief

Advanced Micro Devices

OpenPIC™ Architecture

The emergence of symmetric multiprocessing (SMP) systems in today's high-end PC and server markets has generated a need for new design approaches that achieve optimal performance within this expanded system structure. One of the most significant challenges of multiprocessor system development is the channeling and processing of interrupts.

The answer to that challenge is the OpenPIC™ architecture, a standardized interrupt system that allows systems to share one set of system software drivers. A standardized approach provides opportunity for market growth and reduces the cost and complexity of SMP system development.

The new OpenPIC architecture, jointly developed by AMD and Cyrix, offers an open architecture solution that can meet the requirements of today's higher-performance multiprocessor applications. Designed as an open SMP interrupt controller solution, this architecture supports all current x86 vendors' products, offers a common interface, and provides a compatible, superior successor to the 8259 interrupt controller standard.

The growing prevalence of multimedia components and use of the PCI local bus in typical desktop and server systems threatens to overload interrupt resources, especially in I/O-intensive servers. The OpenPIC specification provides a flexible solution to interrupt overloading. By distributing interrupts to multiple CPUs, the OpenPIC specification greatly expands the number of interrupt channels available to system peripherals, overcoming the interrupt-handling limitations inherent in standard interrupt controllers.

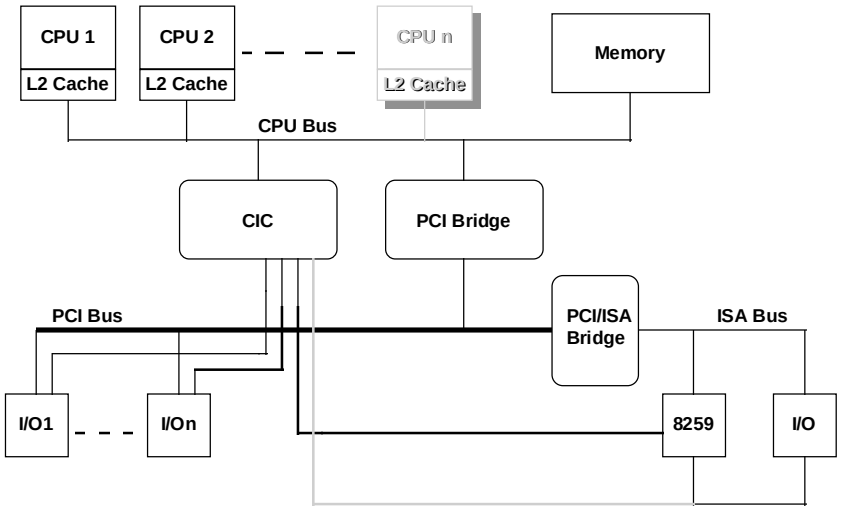
The emergence of the OpenPIC architecture yields multiple benefits. It reduces the number of SMP interrupt controller interfaces system software must support. It gives better access to SMP technology for all applications. The architecture supports a simplified installation and update process for hardware and software. Because it is an open architecture, the likelihood of future support for current software is maximized and costs associated with proprietary development or royalties are eliminated. Finally, as multiple-x86 CPU vendors begin to support the OpenPIC specification, system designers can be free to focus their efforts on the development of new applications and increasing the overall performance of SMP systems.

Features:

- ❑ Flexible number of processors supported up to a maximum of 32
- ❑ Flexible number of interrupt sources supported up to a maximum of 2048
- ❑ Supports the connection of an external 8259 pair for ISA/AT compatibility
- ❑ Multicast capable interprocessor interrupts
- ❑ Processor initialization control
- ❑ Basic interrupt delivery method: directed
- ❑ Advanced delivery mode for distributed interrupts
- ❑ Four global high resolution timers
- ❑ Feature reporting mechanism includes number of processors and interrupt sources supported
- ❑ Flexible feature expansion
- ❑ All registers are 32 bits and are aligned on 128 bit boundaries for 32/64/128 bit bus operation
- ❑ Register blocks aligned on 4K boundaries to allow the mapping of registers to distinct memory pages

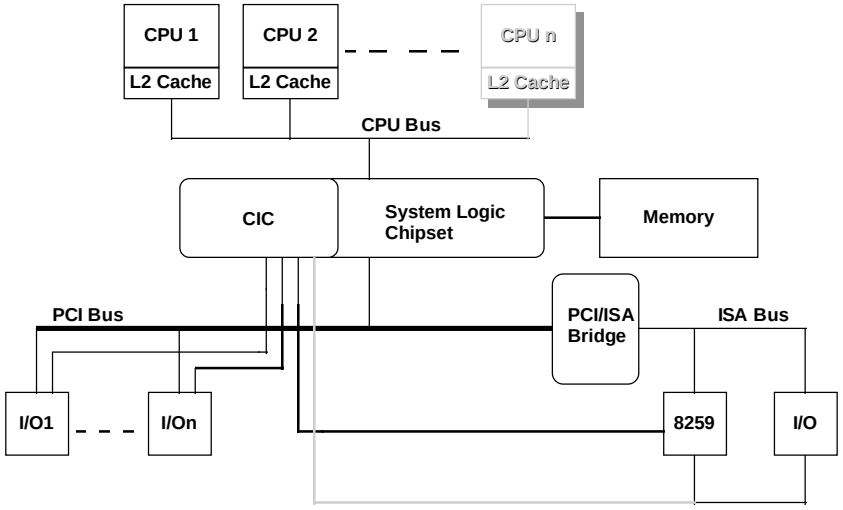
Request additional information via e-mail at openpic@amd.com.

Stand-Alone Controller Example



In this PCI-based system example, a centralized interrupt controller (CIC), which supports the OpenPIC architecture features and register set, is implemented as a stand-alone device. It resides on the CPU/Memory Bus (or Multiprocessing Bus). All interrupt sources are connected to the CIC. The ISA Bus 8259 interrupt controller pair output is also connected to the CIC to enable the pass through mode for start-up AT compatibility.

Integrated Controller Example



In this example system, a centralized interrupt controller (CIC), which supports the OpenPIC architecture features and register set, is integrated into the system logic chipset. As part of the system logic, it has access (internal connection capability) to both the CPU/Memory bus and the PCI bus. It resides on the CPU/Memory Bus (or Multiprocessing Bus). All interrupt sources are connected to the CIC. The ISA Bus 8259 interrupt controller pair output is also connected to the CIC to enable the pass through mode for start-up AT compatibility.

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Please include your name, title, company name, address, and telephone number with your request.